High Level Synthesis Of ASICs Under Timing And Synchronization Constraints (The Springer International Series In Engineering And Computer Science) By David C. Ku

By David C. Ku

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ED&TC 96 0-89791-821/96 $5.00 1996 IEEE High-Level Synthesis of Gracefully Degradable ASICs Wah Chan Alex Orailoglu Dept. of Electrical and Computer Engineering

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high-level synthesis works at a higher level of abstraction, starting with an algorithmic description in a high-level language such as SystemC and Ansi C/C++.

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High level synthesis techniques for the synthesis of restructurable dutapaths are introduced. The techniques can be used in applications such as design for fault

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Lecture Notes In Computer Science design is done under multiple constraints systems poses some new challenges for high-level synthesis

1. David Ku was born in Tapei, Taiwan, in April 1964. He received in 1986 the BS degree in Electrical Engineering, Summa cum Laude, and the BS degree in Computer

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