

High Level Synthesis Of ASICs Under Timing And Synchronization Constraints (The Springer International Series In Engineering And Computer Science) By David C. Ku

By David C. Ku

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High Level Synthesis of ASICs Under Timing and Synchronization Constraints / David C. Ku, High Level Synthesis of ASICs Under Timing Computer-aided synthesis

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High level synthesis techniques for the synthesis of restructurable dutapaths are introduced. The techniques can be used in applications such as design for fault

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high-level synthesis works at a higher level of abstraction, starting with an algorithmic description in a high-level language such as SystemC and Ansi C/C++.

of commercial high-level synthesis timing, concurrency, synchronization, degree in electrical engineering and computer science from the

The translate phase merges all the synthesized netlists and the physical and timing constraints to placing a high-engineering A. High-level Synthesis

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Today, high-level synthesis, also known as ESL synthesis and behavioral synthesis, Software tools for logic synthesis targeting ASICs

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