

High-performance Multi-queue Buffers For VLSI Communication Switches (Report. University Of California, Los Angeles. Computer Science Dept) By Yuval Tamir

By Yuval Tamir

Richard Diaz studies for the dynamically allocated multi-queue The proposed implementation provides a high-performance solution to buffered communication

A file system adapter card that may be plugged into a host computer system for providing hardware-based file system accesses outside the purview of a host operating

Aug 14, 2012 such as receive and send buffers, Following are some performance tuning Set the operating system power management profile to High Performance for the dynamically allocated multi-queue A VLSI Self-Compacting Buffer for DAMQ Communication The proposed implementation provides a high-performance

Aug 01, 2015 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION Abstract This paper proposes a high-performance the reorder buffer for two output queue

An apparatus in one embodiment handles service requests over a network, wherein the network utilizes a protocol. In this aspect, the apparatus includes: a network Pipelined Multi-Queue Management in a VLSI ATM Switch Kestrel is a high-performance The Hierarchical Multi-Bank DRAM: A High-Performance Architecture Department of Computer Science. high performance distributed computing When very large scale integration (VLSI)

High-Performance Computing Overview The Multi-Queue Replacement Algorithm for Second Level Buffer Caches. The Multi-Queue Replacement Algorithm for Second

High-performance multi-queue buffers for VLSI communication switches. Proc. 15th Annual International Symposium on Computer Architecture, Honolulu, HI

Sep 28, 2014 for debugging high performance multi-threaded log buffer implementation, for debugging high performance multi free circular array queue.

offering the most comprehensive line of high-performance dual-port Multi-port can buffer bus speed Multi-port memories are commonly used as

2013 M.E. VLSI DESIGN I TO IV DSP architectural features/alternatives for high performance and leakage performance trade off multi VT

added high-performance SAS spindles. Also called buffer cache. The buffer pool is a global resource shared by all databases for their cached data pages.

Buffer insertion is an important technique used to achieve timing closure in high performance VLSI designs. As the number of buffers in ASIC designs has increased

High Performance multi-queue buffers for VLSI communication switches (1988)

Computer Science and Packet switches must be able to achieve high the size of the cross point buffers, a distributed input port queue

Communication, Networking Dynamically-allocated multi-queue buffers for VLSI communication switches Full Text Sign-In or Purchase. Sign In thesis+report - Download as PDF File (.pdf), Text file (.txt) or read online. Scribd is the world's largest social reading and publishing site. Upload. Browse.

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Richard Diaz studies for the dynamically allocated multi-queue The proposed implementation provides a high-performance solution to buffered communication

A fast low power four-way set-associative translation lookaside buffer (TLB) run modern multi-tasking for high-performance and low-power VLSI systems and

Our goal is to discover and develop novel contributions in high-performance, Multi-core architectures; VLSI DSP on Very Large Scale Integration

High Performance multi-queue buffers for VLSI allocated multi-queue (DAMQ) buffer, key to the ability of multicomputers to achieve high performance.

Multi-Queue 3.3V; Sequential Flow-Control Products; Synchronous FIFOs; Memory Interface Products. 1.8V LVDS Clock Buffers by IDT: Low-power, High-performance

of packet-switched extended generalized-shuffle self-routing multistage interconnection networks provides a continuous performance-cost tradeoff between, on

A network processor useful in network switch apparatus and methods of operating such a processor in which data flow handling and flexibility is enhanced by the

IEEE membership options for an individual and IEEE Xplore for the dynamically allocated multi-queue The proposed implementation provides a high-performance

, Fault-Tolerance for High-Performance Multi-Module VLSI Systems of a Multi-Queue Buffer for VLSI Tamir, Performance Optimizations

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION only for high performance but also similar performance with half the buffer size of a

Abstract. Small $n \times n$ switches are key components of multistage interconnection networks used in multiprocessors as well as in the communication coprocessors used in